Abstract

A system and method are provided for compensating for output error in a sigma delta circuit. The system includes an input for receiving an input signal and an output configured to output a output signal. The system further includes a summation component configured to add a first error voltage value, which is derived from an output signal, to an incoming input signal, and a subtraction component configured to subtract a second error voltage value, where the second error voltage value is derived from the adding of a first error voltage value to an incoming input signal.